a trench formed in said epitaxial layer extending from said top surface of said epitaxial layer through said source and body regions to a depth d_{tr}, said depth d_{tr} being less than said depth d_{max}, said trench being closer to said second point than said first point.

16. A trench DMOS transistor cell as in Claim 17, wherein said body region has a portion exposed at said top surface of said epitaxial layer.

18. A trench DMOS transistor cell as in Claim 18, wherein said source region has a portion exposed at said top surface of said epitaxial layer.

20. A trench DMOS transistor cell as in Claim 17, wherein depth d_{tr} is less than d_{max} by an amount sufficient to cause semiconductor surface breakdown to occur at a point closer to said first point than said second point.

21. A trench DMOS transistor cell as in Claim 17, wherein said epitaxial layer has a thickness d_{epi} small enough to cause semiconductor surface breakdown to occur at a point closer to said first point than said second point.

22. A trench DMOS transistor cell as in Claim 17, wherein said trench, when viewed from above said top surface of said epitaxial structure, is polygonal, having a number of sides greater than four.

23. A trench DMOS transistor cell as in Claim 22, wherein said number of sides is six.

24. A trench DMOS transistor cell as in Claim 17, wherein said epitaxial layer has a thickness d_{epi}, said depth d_{epi} being

LAW OFFICES OF
SKJERVEN, MORRILL,
MacPHERSON, FRANKLIN
& FRIEL

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 283-1222
FAX (408) 283-1233